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PTO/SB/05 (4/98)
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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 C.F.R. § 1.53(b))

Attorney Docket No.	MIO 051 PA
First Inventor or Application Identifier	Joseph M. Brand
Title	ENCAPSULANT LOCK FEATURE
Express Mail Label No.	EL452892043US

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

ADDRESS TO: **Assistant Commissioner for Patents, Box Patent Application, Washington, DC 20231**

1. [X] * Fee Transmittal Form *(e.g., PTO/SB/17)* *(Submit an original and a duplicate for fee processing)*
2. [X] Specification [*Total Pages* 23]
   (preferred arrangement set forth below)
   - Descriptive title of the Invention
   - Cross References to Related Applications
   - Statement Regarding Fed sponsored R & D
   - Reference to Microfiche Appendix
   - Background of the Invention
   - Brief Summary of the Invention
   - Brief Description of the Drawings *(if filed)*
   - Detailed Description
   - Claim(s)
   - Abstract of the Disclosure
3. [X] Drawing(s) *(35 U.S.C. 113)* [*Total Sheets* 2]
4. Oath or Declaration [*Total Pages* 1]
   a. [X] Newly executed (original or copy)
   b. [ ] Copy from a prior application (37 C.F.R. § 1.63(d)) *(for continuation/divisional with Box 16 completed)*
      i. [ ] DELETION OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 C.F.R. §§ 1.63(d)(2) and 1.33(b).

NOTE FOR ITEMS 1 & 13: IN ORDER TO BE ENTITLED TO PAY SMALL ENTITY FEES, A SMALL ENTITY STATEMENT IS REQUIRED (37 C.F.R. § 1.27), EXCEPT IF ONE FILED IN A PRIOR APPLICATION IS RELIED UPON (37 C.F.R. § 1.28).

5. [ ] Microfiche Computer Program *(Appendix)*
6. Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all necessary)*
   a. [ ] Computer Readable Copy
   b. [ ] Paper Copy (identical to computer copy)
   c. [ ] Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

7. [X] Assignment Papers (cover sheet & document(s))
8. [X] 37 C.F.R.§3.73(b) Statement *(when there is an assignee)* [X] Power of Attorney
9. [ ] English Translation Document *(if applicable)*
10. [ ] Information Disclosure Statement (IDS)/PTO-1449 [ ] Copies of IDS Citations
11. [ ] Preliminary Amendment
12. [X] Return Receipt Postcard (MPEP 503) *(Should be specifically itemized)*
13. [ ] * Small Entity Statement(s) *(PTO/SB/09-12)* [ ] Statement filed in prior application, Status still proper and desired
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15. [X] Other: Check $1738.00 (filing fee); Check $40.00 (assignment); Initial Information Data Sheet

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17. CORRESPONDENCE ADDRESS

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Initial Information Data Sheet

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Application Information

Title Line One::	ENCAPSULANT LOCK FEATURE
Total Drawing Sheets::	2
Formal Drawings?::	Yes
Application Type::	Utility
Docket Number::	MIO 051 PA

Representative Information

Registration Number One::	26,397
Registration Number Two::	27,262
Registration Number Three::	29,001
Registration Number Four::	28,046
Registration Number Five::	33,579
Registration Number Six::	39,564
Registration Number Seven::	38,769
Registration Number Eight::	40,830
Registration Number Nine::	33,758
Registration Number Ten::	30,871
Registration Number Eleven::	34,095

ENCAPSULANT LOCK FEATURE

BACKGROUND OF THE INVENTION

The present invention relates to semiconductor die encapsulation and, more particularly, to an encapsulation scheme that provides for improved adhesion of the encapsulant to an underlying printed circuit board.

Plastic encapsulates are commonly used in integrated circuit packaging to protect the integrity of the encapsulated semiconductor die and the associated electrical connections. U.S. Patent No. 5,701,034 (Marrs) is directed to providing improved encapsulation of a semiconductor die and teaches the formation of a locking moat in a heat sink to which the semiconductor die is coupled. The encapsulant material is cured in the locking moat of the heat sink and about the semiconductor die to interlock the encapsulant and the heat sink. The teachings of U.S. Patent No. 5,701,034 are not, however, related to improving adhesion or coupling of the encapsulant to resin laminates commonly utilized to form printed circuit boards. Further, the design of the locking moats and the structure of the heat sink in the '034 patent do not complement each other to provide for an efficient method of manufacture.

In many instances, a semiconductor die is positioned on the upper surface of a printed circuit board substrate and an encapsulant is arranged to cover the semiconductor die, portions of the upper surface of the substrate, and any leads, bond pads, or other bonding locations on the upper surface of the substrate. Robust encapsulant-to-substrate adhesion is critical in this type of structure because the encapsulant contacts only the upper surface of the substrate, as opposed to completely surrounding the substrate and die.

In practice, encapsulant-to-substrate adhesion is limited by specific design constraints. For example, the upper surface of the substrate typically includes conductive portions and solder resist portions. It is often difficult to identify a suitable encapsulant that bonds equally well to the conductive portions and the solder resist

portions. Further, the encapsulant material must also be selected to minimize the deleterious effects of particulate matter contaminating the surface of the substrate. All of these design considerations limit the ability to achieve sufficient encapsulant-to-substrate adhesion.

Accordingly, there is a need for a semiconductor die encapsulation scheme that provides for optimum encapsulant-to-substrate adhesion while accounting for variations in the composition of the substrate surface and for the deleterious effects of particulate matter on the surface of the substrate, particularly where the substrate involved is a printed circuit board laminate. Further, there is a need in the art for an encapsulation scheme that is directed to improving adhesion or coupling of the encapsulant to the resin laminates commonly utilized to form printed circuit boards.

BRIEF SUMMARY OF THE INVENTION

This need is met by the present invention wherein a void is formed in the structure of a laminate supporting a semiconductor die and where an encapsulant is arranged to encapsulate the semiconductor die and fill the void in the laminate.

In accordance with one embodiment of the present invention, a packaged semiconductor device is provided comprising a semiconductor chip, a laminate, and an encapsulant. The laminate defines first and second major faces and includes an electrically conductive layer, an underlying substrate supporting the electrically conductive layer, and at least one void formed in the laminate so as to extend from one of the major faces through the electrically conductive layer at least as far as the underlying substrate. The encapsulant is positioned to mechanically couple the semiconductor die to the laminate to extend into the void so as to contact the underlying substrate.

The void or voids preferably extend into the underlying substrate and may extend from the first major face through the electrically conductive layer and the underlying

substrate to the second major face. The contact between the encapsulant and the underlying substrate is preferably characterized by an adhesive bond and the encapsulant preferably occupies substantially all of the void.

In accordance with another embodiment of the present invention, a packaged semiconductor device is provided comprising a semiconductor chip, a laminate, and an encapsulant. The laminate defines first and second major faces and includes a solder resist layer, an underlying substrate, an electrically conductive layer interposed between the solder resist layer and the underlying substrate, and at least one void formed in the laminate so as to extend from one of the major faces through the solder resist layer and the electrically conductive layer at least as far as the underlying substrate. The encapsulant is positioned to mechanically couple the semiconductor die to the laminate and to extend into the void so as to contact the underlying substrate.

In accordance with yet another embodiment of the present invention, a packaged semiconductor device is provided comprising a semiconductor chip, a laminate, and an encapsulant. The laminate defines first and second major faces and includes a plurality of laminated layers. The laminate also includes at least one void formed therein so as to extend from one of the major faces through a plurality of the laminated layers. The encapsulant is positioned to mechanically couple the semiconductor die to the laminate and is further positioned to extend into the void across the plurality of laminated layers so as to contact a portion of the laminate between the first and second major faces of the laminate.

In accordance with yet another embodiment of the present invention, a packaged semiconductor device is provided comprising a semiconductor chip, a prepreg epoxy resin glass-cloth laminate, and an encapsulant. The prepreg epoxy resin glass-cloth laminate defines first and second major faces and includes a plurality of laminated prepreg layers and at least one void formed therein so as to extend from one of the major faces through a plurality of the laminated prepreg layers. The encapsulant is positioned to mechanically couple the semiconductor die to the prepreg epoxy resin

glass-cloth laminate and to extend into the void across the plurality of laminated prepreg layers so as to contact a portion of the laminate between the first and second major faces of the laminate.

In accordance with yet another embodiment of the present invention, a packaged semiconductor device is provided comprising a semiconductor chip, a laminate, and an encapsulant. The laminate defines first and second major faces and includes a plurality of laminated layers and at least one void formed therein so as to extend from one of the major faces through a plurality of the laminated layers. The void is characterized by a profile that varies across adjacent laminated layers. The encapsulant is positioned to mechanically couple the semiconductor die to the laminate and to extend into the void across the varying profile so as to contact a portion of the laminate between the first and second major faces of the laminate. The varying profile may be characterized by a cross-sectional area that changes from a first value in a selected laminated layer to a second value in an adjacent laminated layer. The second value is preferably larger than the first value.

In accordance with yet another embodiment of the present invention, a packaged semiconductor device is provided comprising a semiconductor chip, a laminate, and an encapsulant. The laminate defines first and second major faces and includes a plurality of laminated layers, including a selected laminated layer and an adjacent laminated layer. The selected laminated layer is disposed closer to the first major face than the adjacent laminated layer. The laminate includes at least one void formed therein so as to extend from the first major face through the selected laminated layer and into the adjacent laminated layer. The void is characterized by a varying profile that defines a ledge portion in the selected laminated layer and an underlying cavity in the adjacent laminated layer. An encapsulant is positioned to mechanically couple the semiconductor die to the laminate and to extend into the void across the ledge portion into the underlying cavity so as to contact a portion of the laminate between the first and second major faces of the laminate. The selected laminated layer may comprise a

plurality of laminated layers. Similarly, the adjacent laminated layer may comprise a plurality of laminated layers.

In accordance with yet another embodiment of the present invention, a packaged semiconductor device is provided comprising a semiconductor chip, a laminate, and an encapsulant. The laminate defines first and second major faces and includes a plurality of laminated layers and at least one void formed therein so as to extend from one of the major faces through a plurality of the laminated layers. The void is characterized by a cross-sectional area that changes from a first value in a selected laminated layer to a second value in an adjacent laminated layer. The encapsulant is positioned to mechanically couple the semiconductor die to the laminate, wherein the encapsulant is further positioned to extend into the void across the varying cross-sectional area.

In accordance with yet another embodiment of the present invention, an encapsulated integrated circuit is provided comprising a semiconductor die, a printed circuit board, and an encapsulant. The printed circuit board is conductively coupled to the semiconductor die and comprises a laminate defining first and second major faces. The laminate includes a solder resist layer, an underlying substrate, an electrically conductive layer interposed between the solder resist layer and the underlying substrate, and at least one void formed in the printed circuit board so as to extend from one of the major faces through the solder resist layer and the electrically conductive layer at least as far as the underlying substrate. The encapsulant is positioned to mechanically couple the semiconductor die to the printed circuit board and to extend into the void.

In accordance with yet another embodiment of the present invention, a computer is provided including at least one packaged semiconductor device comprising a semiconductor chip, a laminate, and an encapsulant. The laminate defines first and second major faces and includes an electrically conductive layer, an underlying substrate supporting the electrically conductive layer, and at least one void formed in the laminate so as to extend from one of the major faces through the electrically

conductive layer at least as far as the underlying substrate. The encapsulant is positioned to mechanically couple the semiconductor die to the laminate and to extend into the void so as to contact the underlying substrate.

In accordance with yet another embodiment of the present invention, an epoxy resin glass-cloth laminate is provided comprising first and second major faces, and a plurality of laminated epoxy resin glass-cloth layers. The second major face is oriented substantially parallel to the first major face. The plurality of laminated epoxy resin glass-cloth layers define a portion of the laminate between the first and second major faces. The laminate includes at least one void formed therein so as to extend from one of the major faces through a plurality of the laminated layers. The void is characterized by a profile that varies across adjacent laminated layers. The laminated layers preferably comprise bismaleimide triazine resin.

In accordance with yet another embodiment of the present invention, an encapsulated integrated circuit is provided comprising a semiconductor die, a printed circuit board, and an encapsulant. The printed circuit board is conductively coupled to the semiconductor die and comprises a laminate defining first and second major faces. The laminate includes a solder resist layer, an electrically conductive layer, and a bismaleimide triazine resin laminate including a selected laminated layer and an adjacent laminated layer. The electrically conductive layer is interposed between the solder resist layer and the underlying substrate. The selected laminated layer is disposed closer to the first major face than the adjacent laminated layer. The laminate includes at least one void formed therein so as to extend from one of the major faces through the solder resist layer and the electrically conductive layer at least as far as the adjacent laminated layer. The void is characterized by a varying profile that defines a ledge portion in the selected laminated layer and an underlying cavity in the adjacent laminated layer. The encapsulant is positioned to mechanically couple the semiconductor die to the printed circuit board and to extend through the void into the underlying cavity so as to form an adhesive bond with the bismaleimide triazine resin

laminate. The semiconductor die is supported by the bismaleimide triazine resin laminate and the encapsulant and the bismaleimide triazine resin laminate are arranged to enclose substantially all of the semiconductor die.

In accordance with yet another embodiment of the present invention, a method of encapsulating an integrated circuit is provided comprising the steps of (i) providing a semiconductor chip; (ii) providing a laminate defining first and second major faces, the laminate including an electrically conductive layer, and an underlying substrate supporting the electrically conductive layer; (iii) forming at least one void in the laminate so as to extend from one of the major faces through the electrically conductive layer at least as far as the underlying substrate; and (iv) encapsulating the semiconductor die and the laminate with an encapsulant such that the encapsulant extends into the void to contact the underlying substrate.

In accordance with yet another embodiment of the present invention, a method of forming an epoxy resin glass-cloth laminate is provided and comprises a process of laminating a plurality of epoxy resin glass-cloth layers such that the laminate includes at least one void formed therein extending from one of the major faces through a plurality of the laminated layers, and such that the void is characterized by a profile that varies across adjacent laminated layers.

Accordingly, it is an object of the present invention to provide a packaged semiconductor device or encapsulated integrated circuit, a computer including a packaged semiconductor device, a method of encapsulating an integrated circuit, and a method of forming an epoxy resin glass-cloth laminate whereby an encapsulant may be arranged to encapsulate a semiconductor die and fill a void formed in the structure of a laminate supporting the semiconductor die. Other objects of the present invention will be apparent in light of the description of the invention embodied herein.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS

The following detailed description of the preferred embodiments of the present invention can be best understood when read in conjunction with the following drawings, where like structure is indicated with like reference numerals and in which:

Fig. 1 is a schematic cross-sectional illustration of an encapsulated semiconductor die package according to the present invention;

Fig. 2 is a schematic, broken away, cross-sectional illustration of a portion of a encapsulated semiconductor die package according to one embodiment of the present invention;

Fig. 3 is a schematic, broken away, cross-sectional illustration of a portion of a encapsulated semiconductor die package according to an alternative embodiment of the present invention; and

Fig. 4 is an exploded view of the encapsulated semiconductor die package illustrated in Fig. 3.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring now to Figs. 1 and 2, a packaged semiconductor device or encapsulated integrated circuit 10 according to the present invention comprises a semiconductor die or chip 20, a printed circuit board laminate 30 conductively coupled to the semiconductor die 20 (electrical connections not shown), and an encapsulant 40.

The printed circuit board laminate 30 comprises a laminate defining a first major face 31 and a second major face 32. At its first major face 31, the laminate includes a solder resist layer 34, an electrically conductive layer 36, and an underlying resin laminate substrate 38 supporting the electrically conductive layer 36 and the solder resist layer 34. In the illustrated embodiment, the printed circuit board laminate 30 includes an additional solder resist layer 34 and an additional electrically conductive layer 36 at the second major face 32 of the printed circuit board laminate 30.

The resin laminate 38 of the printed circuit board laminate 30 is preferably a prepreg epoxy resin glass-cloth laminate, e.g., a BT laminate (bismaleimide triazine), an FR-4 epoxy-glass laminate, an FR-5 epoxy-glass laminate, or another suitable laminate structure. The resin laminate 38 includes a plurality of adjacent laminated layers 38A-38F. The nature and extent of each laminated layer is perhaps best illustrated in the exploded view illustration of Fig. 4.

A void 50 is formed in the printed circuit board laminate 30 and extends from the first major face 31, through the plurality of adjacent laminated layers 38A-38F, to the second major face 32. The encapsulant 40 is positioned to mechanically couple the semiconductor die 20 to the printed circuit board laminate 30 by extending into the void 50 across the plurality of laminated layers 38A-38F. The resulting contact between the encapsulant 40 and the interior portion of the printed circuit board laminate 30 is characterized by an adhesive bond that solidifies the structure of the encapsulated integrated circuit 10. Preferably, the encapsulant 40 occupies substantially all of the void 50. Further, the encapsulant 40 and the printed circuit board laminate 30 enclose substantially all of the semiconductor die 10.

Referring now to Figs. 3 and 4, an alternative embodiment of the present invention is illustrated. In the embodiment of Figs. 3 and 4, the void 50 is characterized by a profile that varies across the plurality of adjacent laminated layers 38A-38F. The encapsulant 40 (not shown in Figs. 3 and 4) is arranged to extend into the void 50 across the varying profile. In this manner, the varying profile functions to further secure the encapsulant within the void 50 and further solidify the mechanical coupling between the semiconductor die 20 and the printed circuit board laminate 30.

In the illustrated embodiment, the varying profile of the void 50 defines a ledge portion 60 in the selected laminated layers 38A, 38B and an underlying cavity 62 in the adjacent laminated layer 38C such that the varying profile of the void 50 is characterized by a cross-sectional area that changes from a first value in the selected laminated layers 38A, 38B to a larger value in the adjacent laminated layer 38C. Although, in the illustrated embodiment, two laminated layers 38A, 38B define the ledge portion 60 and a single laminated layer 38C defines the underlying cavity 62 , it is contemplated by the present invention that any number of layers may be selected to form the ledge portion 60 and the underlying cavity 62. Further, although a simple T-shaped profile is illustrated in Figs. 3 and 4, it is contemplated by the present invention that a variety of varying profiles may be utilized to accomplish the objectives of the present invention.

As will be appreciated by those practicing the present invention the method of encapsulating the integrated circuit or semiconductor die 20 comprises the steps of: (i) providing the semiconductor die 20; (ii) providing the printed circuit board laminate 30; (iii) forming the void 50 in the laminate 30 such that it extends at least as far as the underlying resin laminate substrate 38; and (iv) encapsulating the semiconductor die 20 and the laminate 30 with an encapsulant 40 such that the encapsulant 40 extends into the void to contact the underlying substrate 38. As will be further appreciated by those practicing the present invention, a variety of methods are available for forming the void 50. For example, the void 50 may be formed by drilling, stamping, or chemical etching.

Further, it is contemplated by the present invention that the varying profile of the void 50 within the resin laminate substrate 38 may be provided by processing separately individual ones of the plurality of adjacent laminated layers 38A-38F with respective portions of the void 50 formed in selected ones of the layers 38A-38F. Subsequently, the respective void portions of each layer are aligned to formed the desired profile and joined into a unified resin laminate substrate 38.

Having described the invention in detail and by reference to preferred embodiments thereof, it will be apparent that modifications and variations are possible without departing from the scope of the invention defined in the appended claims.

What is claimed is:

CLAIMS

1. A packaged semiconductor device comprising:

a semiconductor chip;

a laminate defining first and second major faces, said laminate including

an electrically conductive layer,

an underlying substrate supporting said electrically conductive layer, and

at least one void formed in said laminate so as to extend from one of said major faces through said electrically conductive layer at least as far as said underlying substrate; and

an encapsulant positioned to mechanically couple said semiconductor die to said laminate, wherein said encapsulant is further positioned to extend into said void so as to contact said underlying substrate.

2. A packaged semiconductor device as claimed in claim 1 wherein said at least one void extends into said underlying substrate.

3. A packaged semiconductor device as claimed in claim 1 wherein said at least one void extends from said first major face through said ~~elect~~rically conductive layer and said underlying substrate to said second major face and wherein said encapsulant is positioned to extend through said void from said first major face to said second major face.

4. A packaged semiconductor device as claimed in claim 1 wherein said contact between said encapsulant and said underlying substrate is characterized by an adhesive bond.

5. A packaged semiconductor device as claimed in claim 1 wherein said encapsulant occupies substantially all of said void.

6. A packaged semiconductor device as claimed in claim 1 wherein said semiconductor chip is supported by said laminate and wherein said encapsulant and said laminate are arranged to enclose substantially all of said semiconductor chip.

7. A packaged semiconductor device comprising:

a semiconductor chip;

a laminate defining first and second major faces, said laminate including

a solder resist layer,

an underlying substrate,

an electrically conductive layer interposed between said solder resist layer and said underlying substrate, and

at least one void formed in said laminate so as to extend from one of said major faces through said solder resist layer and said electrically conductive layer at least as far as said underlying substrate; and

an encapsulant positioned to mechanically couple said semiconductor die to said laminate, wherein said encapsulant is further positioned to extend into said void so as to contact said underlying substrate.

8. A packaged semiconductor device comprising:

a semiconductor chip;

a laminate defining first and second major faces and including a plurality of laminated layers, said laminate including at least one void formed therein so as to extend from one of said major faces through a plurality of said laminated layers; and

an encapsulant positioned to mechanically couple said semiconductor die to said laminate, wherein said encapsulant is further positioned to extend into said void across said plurality of laminated layers so as to contact a portion of said laminate between said first and second major faces of said laminate.

9. A packaged semiconductor device as claimed in claim 8 wherein said at least one void extends from said first major face through said laminate to said second major face and wherein said encapsulant is positioned to extend through said void from said first major face to said second major face.

10. A packaged semiconductor device as claimed in claim 8 wherein said contact between said encapsulant and said laminate is characterized by an adhesive bond.

11. A packaged semiconductor device as claimed in claim 8 wherein said encapsulant occupies substantially all of said void.

12. A packaged semiconductor device as claimed in claim 8 wherein said semiconductor chip is supported by said laminate and wherein said encapsulant and said laminate are arranged to enclose substantially all of said semiconductor chip.

13. A packaged semiconductor device comprising:

a semiconductor chip;

a prepreg epoxy resin glass-cloth laminate defining first and second major faces and including a plurality of laminated prepreg layers, said prepreg laminate including at least one void formed therein so as to extend from one of said major faces through a plurality of said laminated prepreg layers; and

an encapsulant positioned to mechanically couple said semiconductor die to said prepreg epoxy resin glass-cloth laminate, wherein said encapsulant is further positioned to extend into said void across said plurality of laminated prepreg layers so as to contact a portion of said laminate between said first and second major faces of said laminate.

14. A packaged semiconductor device comprising:

a semiconductor chip;

a laminate defining first and second major faces and including a plurality of laminated layers, said laminate including at least one void formed therein so as to extend from one of said major faces through a plurality of said laminated layers, wherein said void is characterized by a profile that varies across adjacent laminated layers; and

an encapsulant positioned to mechanically couple said semiconductor die to said laminate, wherein said encapsulant is further positioned to extend into said void across said varying profile so as to contact a portion of said laminate between said first and second major faces of said laminate.

15. A packaged semiconductor device as claimed in claim 14 wherein

said laminate includes a selected laminated layer and an adjacent laminated layer,

said selected laminated layer is disposed closer to said first major face than said adjacent laminated layer,

said void extends from said first major face through said selected laminated layer and into said adjacent laminated layer, and

said varying profile defines a ledge portion in said selected laminated layer and an underlying cavity in said adjacent laminated layer.

16. A packaged semiconductor device as claimed in claim 14 wherein said varying profile is characterized by a cross-sectional area that changes from a first value in a selected laminated layer to a second value in an adjacent laminated layer.

17. A packaged semiconductor device as claimed in claim 16 wherein said second value is larger than said first value.

18. A packaged semiconductor device comprising:

a semiconductor chip;

a laminate defining first and second major faces and including a plurality of laminated layers, including a selected laminated layer and an adjacent laminated layer, wherein

said selected laminated layer is disposed closer to said first major face than said adjacent laminated layer,

said laminate includes at least one void formed therein so as to extend from said first major face through said selected laminated layer and into said adjacent laminated layer, and

said void is characterized by a varying profile that defines a ledge portion in said selected laminated layer and an underlying cavity in said adjacent laminated layer; and

an encapsulant positioned to mechanically couple said semiconductor die to said laminate, wherein said encapsulant is further positioned to extend into said void across said ledge portion into said underlying cavity so as to contact a portion of said laminate between said first and second major faces of said laminate.

19. A packaged semiconductor device as claimed in claim 18 wherein said selected laminated layer comprises a plurality of laminated layers.

20. A packaged semiconductor device as claimed in claim 18 wherein said adjacent laminated layer comprises a plurality of laminated layers.

21. A packaged semiconductor device comprising:

a semiconductor chip;

a laminate defining first and second major faces and including a plurality of laminated layers, said laminate including at least one void formed therein so as to extend from one of said major faces through a plurality of said laminated layers, wherein said void is characterized by a cross-sectional area that changes from a first value in a selected laminated layer to a second value in an adjacent laminated layer; and

an encapsulant positioned to mechanically couple said semiconductor die to said laminate, wherein said encapsulant is further positioned to extend into said void across said varying cross-sectional area.

22. An encapsulated integrated circuit comprising:

a semiconductor die;

a printed circuit board conductively coupled to said semiconductor die, wherein said printed circuit board comprises a laminate defining first and second major faces, said laminate including

a solder resist layer,

an underlying substrate,

an electrically conductive layer interposed between said solder resist layer and said underlying substrate, and

at least one void formed in said printed circuit board so as to extend from one of said major faces through said solder resist layer and said electrically conductive layer at least as far as said underlying substrate; and

an encapsulant positioned to mechanically couple said semiconductor die to said printed circuit board, wherein said encapsulant is further positioned to extend into said void.

23. A computer including at least one packaged semiconductor device comprising:

a semiconductor chip;

a laminate defining first and second major faces, said laminate including

an electrically conductive layer,

an underlying substrate supporting said electrically conductive layer,

at least one void formed in said laminate so as to extend from one of said major faces through said electrically conductive layer at least as far as said underlying substrate; and

an encapsulant positioned to mechanically couple said semiconductor die to said laminate, wherein said encapsulant is further positioned to extend into said void so as to contact said underlying substrate.

24. An epoxy resin glass-cloth laminate comprising:

a first major face;

a second major face oriented substantially parallel to said first major face;

a plurality of laminated epoxy resin glass-cloth layers defining a portion of said laminate between said first and second major faces, wherein said laminate includes at least one void formed therein so as to extend from one of said major faces through a plurality of said laminated layers, and wherein said void is characterized by a profile that varies across adjacent laminated layers.

25. An epoxy resin glass-cloth laminate as claimed in claim 24 wherein

said laminated layers include a selected laminated layer and an adjacent laminated layer,

said selected laminated layer is disposed closer to said first major face than said adjacent laminated layer,

said void extends from said first major face through said selected laminated layer and into said adjacent laminated layer, and

said varying profile defines a ledge portion in said selected laminated layer and an underlying cavity in said adjacent laminated layer.

26. An epoxy resin glass-cloth laminate as claimed in claim 24 wherein said varying profile is characterized by a cross-sectional area that changes from a first value in a selected laminated layer to a second value in an adjacent laminated layer.

27. An epoxy resin glass-cloth laminate as claimed in claim 26 wherein said second value is larger than said first value.

28. An epoxy resin glass-cloth laminate as claimed in claim 24 wherein said laminated layers comprise bismaleimide triazine resin.

29. An encapsulated integrated circuit comprising:

a semiconductor die;

a printed circuit board conductively coupled to said semiconductor die, wherein said printed circuit board comprises a laminate defining first and second major faces, said laminate including

a solder resist layer,

a bismaleimide triazine resin laminate, including a selected laminated layer and an adjacent laminated layer, and

an electrically conductive layer interposed between said solder resist layer and said underlying substrate, wherein

said selected laminated layer is disposed closer to said first major face than said adjacent laminated layer,

said laminate includes at least one void formed therein so as to extend from one of said major faces through said solder resist layer and said electrically conductive layer at least as far as said adjacent laminated layer, and

said void is characterized by a varying profile that defines a ledge portion in said selected laminated layer and an underlying cavity in said adjacent laminated layer; and

an encapsulant positioned to mechanically couple said semiconductor die to said printed circuit board, wherein said encapsulant is further positioned to extend through said void into said underlying cavity so as to form an adhesive bond with said bismaleimide triazine resin laminate, wherein said semiconductor die is supported by said bismaleimide triazine resin laminate, and wherein said encapsulant and said bismaleimide triazine resin laminate are arranged to enclose substantially all of said semiconductor die.

30. A method of encapsulating an integrated circuit comprising the steps of:

providing a semiconductor chip;

providing a laminate defining first and second major faces, said laminate including an electrically conductive layer, and an underlying substrate supporting said electrically conductive layer;

forming at least one void in said laminate so as to extend from one of said major faces through said electrically conductive layer at least as far as said underlying substrate; and

encapsulating said semiconductor die and said laminate with an encapsulant such that said encapsulant extends into said void to contact said underlying substrate.

31. A method of forming an epoxy resin glass-cloth laminate defining a first major face and a second major face oriented substantially parallel to said first major face, said method comprising a process of laminating a plurality of epoxy resin glass-cloth layers such that said laminate includes at least one void formed therein extending from one of said major faces through a plurality of said laminated layers, and such that said void is characterized by a profile that varies across adjacent laminated layers.

ABSTRACT OF THE DISCLOSURE

An encapsulated integrated circuit is provided including a semiconductor die, a printed circuit board, and an encapsulant. The printed circuit board is conductively coupled to the semiconductor die and comprises a laminate defining first and second major faces. The laminate includes a solder resist layer, an electrically conductive layer, and a bismaleimide triazine resin laminate including a selected laminated layer and an adjacent laminated layer. The electrically conductive layer is interposed between the solder resist layer and the underlying substrate. The selected laminated layer is disposed closer to the first major face than the adjacent laminated layer. The laminate includes at least one void formed therein so as to extend from one of the major faces through the solder resist layer and the electrically conductive layer at least as far as the adjacent laminated layer. The void is characterized by a varying profile that defines a ledge portion in the selected laminated layer and an underlying cavity in the adjacent laminated layer. The encapsulant is positioned to mechanically couple the semiconductor die to the printed circuit board and to extend through the void into the underlying cavity so as to form an adhesive bond with the bismaleimide triazine resin laminate. The semiconductor die is supported by the bismaleimide triazine resin laminate and the encapsulant and the bismaleimide triazine resin laminate are arranged to enclose substantially all of the semiconductor die.

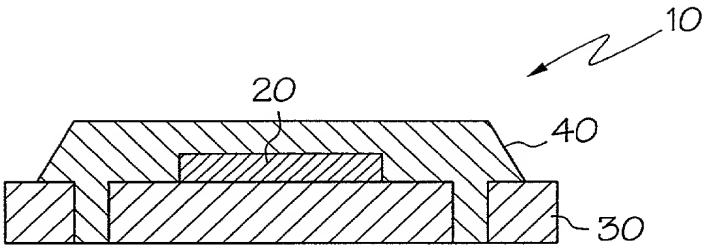

FIG. 1

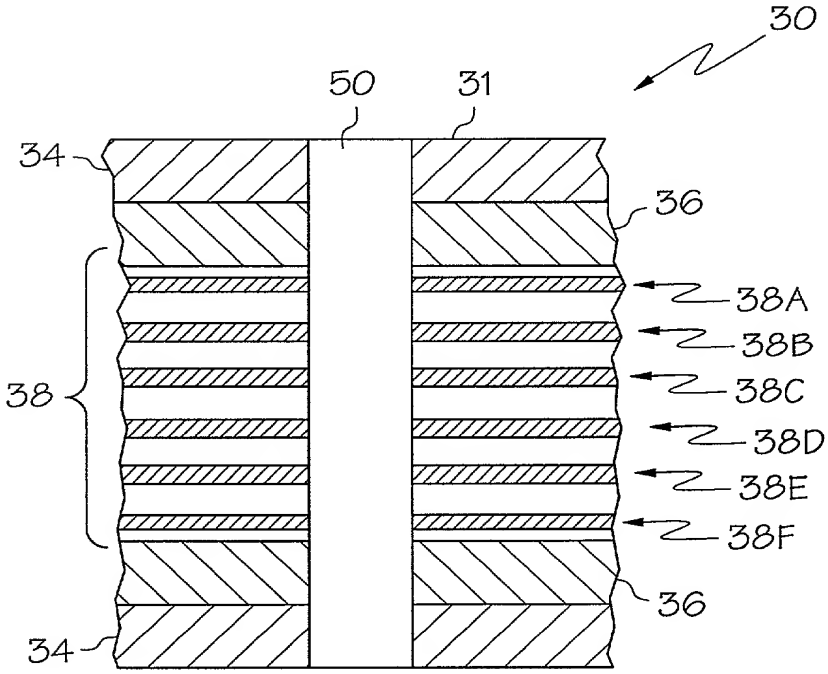

FIG. 2

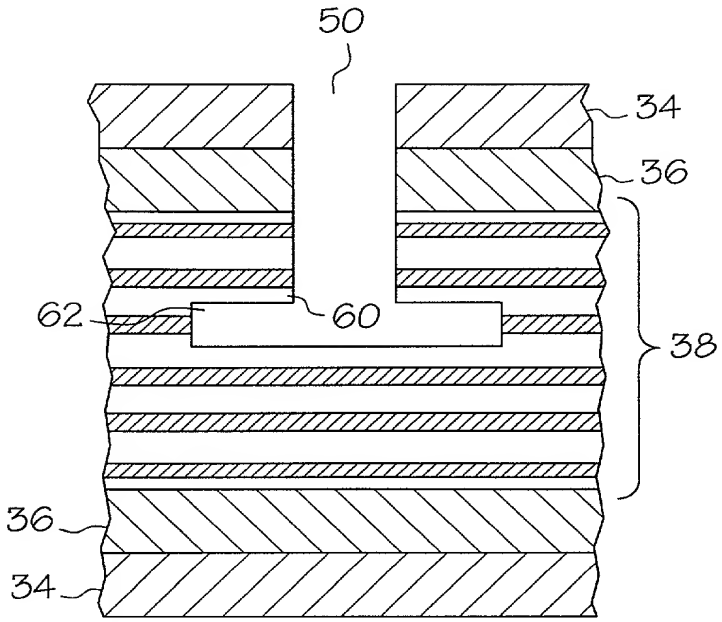

FIG. 3

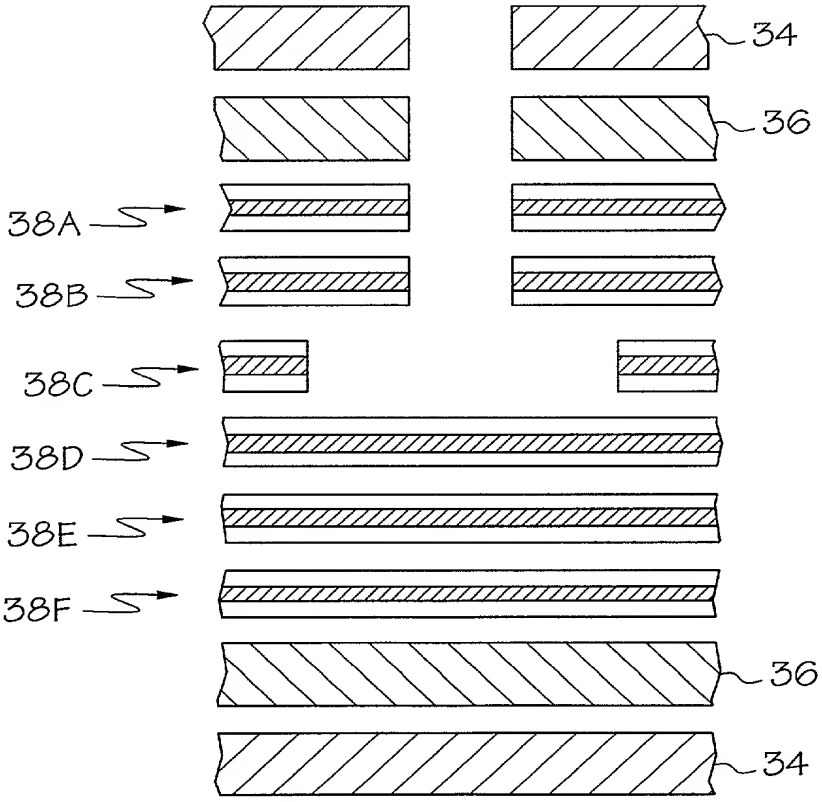

FIG. 4

DECLARATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name; that

I verily believe I am the original, first and sole inventor (if only one name is listed below) or a joint inventor (if plural inventors are named below) of the invention entitled:

ENCAPSULANT LOCK FEATURE (Docket No. MIO 051 PA), described and claimed

__X__ in the attached specification;
_____ in the specification filed _____, as U.S. Application Serial No. _____, and as amended _____.

I hereby authorize the attorney(s) and/or agent(s) appointed herein to indicate above whether the invention is described and claimed in an attached specification and to provide the Filing Date and Serial No. of the corresponding U.S. Application, if previously filed.

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims as filed and as amended by any amendment referred to above.

I acknowledge the duty to disclose to the Patent and Trademark Office all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, §1.56(a).

I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under §1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

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POWER OF ATTORNEY

Applicant: Joseph M. Brand
Application No.: _____ Filed: _____
Entitled: ENCAPSULANT LOCK FEATURE

CERTIFICATE UNDER 37 CFR 3.73(b)

Micron Technology, Inc., a corporation of the State of Delaware, with a place of business at 8000 S. Federal Way, Boise, ID 83706-9632 certifies that it is the assignee of the entire right, title and interest in the patent application identified above by virtue of either:

A. [X] An assignment from the inventor(s) of the patent application identified above, a copy of which is attached.

OR

B. [ ] A chain of title from the inventor(s), of the patent application identified above, to the current assignee as shown below:

1. From: _____ To: _____
   The document was recorded in the Patent and Trademark Office at Reel _____ Frame _____, or for which a copy thereof is attached.

2. From: _____ To: _____
   The document was recorded in the Patent and Trademark Office at Reel _____ Frame _____, or for which a copy thereof is attached.

3. From: _____ To: _____
   The document was recorded in the Patent and Trademark Office at Reel _____ Frame _____, or for which a copy thereof is attached.

[ ] Additional documents in the chain of title are listed on a supplemental sheet.

[ ] Copies of assignments or other documents in the chain of title are attached.

The undersigned has reviewed all the documents in the chain of title of the patent application identified above and, to the best of undersigned's knowledge and belief, title is in the assignee identified above.

The undersigned (whose title is supplied below) is empowered to sign this certificate on behalf of the assignee.

Micron Technology , Inc. hereby appoints the following attorney(s) and/or agent(s) to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith:

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Micron Technology, Inc. hereby declares that all statements made herein of my own knowledge are true, and that all statements made on information and belief are believed to be true; and further, that these statements are made with the knowledge that willful false statements, and the like so made, are punishable by fine or imprisonment, or both, under Section 1001, Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Date: 6-15-99

Name: Michael L. Lynch

Title: Chief Patent Counsel

Signature: